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A Novel Access Scheme for Online Test in RFID Memories

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Abstract - In order to ensure accurate identification and delivery of transponder information, radio frequency identification devices depend on their memory to operate correctly. A novel method of online testing RFIDs is presented in this paper based on March-BIST technology. Online testing is obtained by modifying the access mode of the transponder to take advantage of the waiting time the transponder wastes before it is accessed. We simulated and synthesized the VHDL solution in order to obtain timing and area results. The results show that the solution overhead is lower rather than compared to other available solutions, while the timing performance allows for testing of up to 32-word blocks inside a single waiting slot.

***Key Words*:** RFIDs, BIST, VHDL

1. INTRODUCTION

The rapid development of the very large-scale integrated field (VLSI) has enabled the fabrication of increasing numbers of transistors onto a single silicon die. Although integrated circuits (ICs) can currently be manufactured with over one million gates, this will likely change in the future Test methods have become more sophisticated as chips have become more complex [1].

Therefore, manufacturing testing has the potential to improve the declining manufacturing yield, as well as control the rising production cost resulting from the increasing volume of test data and increased testing times. In order to achieve better product reliability and production yield, reducing the cost of manufacturing tests and improving test quality is already generally accepted as a key task in VLSI design [2].

If a product fails a test after being designed, manufactured, and tested, there must be a reason for the failure. Either the test was erroneous, the fabrication process was flawed, the design was improper, or there was an issue with the specification. Everything is possible to fail. The function of testing is to discover whether something went wrong, but the role of diagnosis is to establish exactly what went wrong and where the process needs to be changed [3].

As a result, the accuracy and efficacy of testing are critical for high-quality products (another name for perfect products.) If the test technique is sound yet the product fails, it is reasonable to mistrust the fabrication process, design, or specification [4].

Testing has two advantages: quality and cost. These two characteristics are not mutually exclusive, and neither can exist without the other. Quality means meeting the user's needs for the least amount of money. All bad products may be weeded out before they reach the user with a good testing method. However, if there are too many bad goods produced, the cost of those bad items must be recovered from the price charged for the few excellent items produced. Without a thorough understanding of the physical concepts behind manufacturing and testing procedures, an engineer will be unable to develop a high-quality product. VLSI chip testing is carried out by a variety of persons at a variety of locations. When a new chip is created and produced for the first time, it should be tested to ensure that the design and test technique are correct. This frequently necessitates the assistance of a design engineer, and testing may even take place in a design lab rather than a factory. Both the design and the test process may be altered as a result of the findings. Verification testing [5] is the term for this.

Productivity rises as quality rises, yet quality inspection is too late, ineffectual, and expensive to enhance quality. There are exceptions, however, where mistakes and duds are unavoidable but unacceptably costly. Manufacturing of complex integrated circuits is, I suppose, one example. The only way out is to separate the good from the bad, thus it's critical to inspect at the proper time to save money overall [6].

External testing with automatic test equipment (ATE) and internal testing with built-in self-test are the two primary methods for testing electronic circuits (BIST). Input test vectors and accurate response data are saved in the ATE memory when external testing is used. The ATPG tools are used to create input test vectors, and circuit simulation is used to collect accurate response data. The comparison is done on the tester [7] for external testing. Although ATE-based test methodologies have previously dominated, the gap between ATE capabilities and circuit test needs is widening as transistor to pin ratios and circuit operating frequencies rise (especially in terms of speed and volume of test data).

2. BIST Techniques

The Logic BIST (LBIST) and the Memory BIST (MBIST) are the two most common BIST techniques (MBIST). In LBIST, which is developed for testing random logic, a pseudo-random pattern generator (PRPG) is used to produce input patterns that are applied to the device's internal scan chain, and a multiple input signature register (MISR) is used to acquire the device's response to these test input patterns. A faulty device is implied by an erroneous MISR result [8].

BIST is quickly emerging as a viable alternative to the rising costs of external electrical testing and the increasing complexity of devices. As more and better BIST approaches are developed, this approach will be used in a larger range of

situations [9]. This does not imply that BIST will someday replace external electrical testing. Still, proponents of BIST believe that it will one day be the preferred form of testing, rather than only an option to external ATE testing as it is now.

In its most basic form, BIST entails designing a circuit such that it can test itself and decide whether it is fault-free or problematic. To support the self-testing capability, additional circuitry and functionality must normally be integrated into the circuit design. This extra capability must be capable of both creating test patterns and determining if the Circuit under Test (CUToutput)'s responses to the test patterns match to those of a fault-free circuit. Figure 1 depicts the basic testing technique.

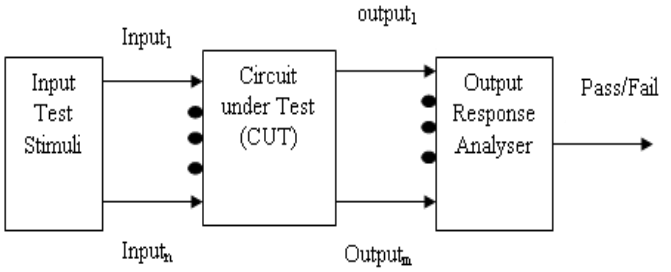

Fig -1: Basic approach of testing

In BIST implementations, signature analysis is the most often utilised approach for ORAs. The fundamental component of the ORA implementation is signature analysis, which employs an LFSR. The signature analysis works by dividing the polynomial representing the CUT's output replies by the characteristic polynomial of the LFSR that was used to perform the ORA.

3. MARCH TEST ALGORITHM

Many methods have been devised for evaluating semi-conductor memory, as demonstrated in the, with the March tests being the most popular and beneficial. A March test consists of a succession of March components, each of which is made of a read/write operation that must be done in every memory cell. March testing may identify a variety of fault types, including Stuck-at Faults (SAF), Address Faults (AF), and certain Coupling Faults (CF).

Figure 2 depicts how this notation is interpreted for MATS++ as a testing algorithm. Word-oriented memories, such as those found in RFID tags, need a somewhat different technique. March approach may be simply adapted to RFID's word-oriented memory with a reduction in CF coverage by expanding the 0 or 1 to 16 bits.

Figure 2 depicts the MATS++ March test's behaviour when cell (2, 1) suffers a SA0 fault. MATS++ has the March components M0, M1, and M2. March element M2 detects the problem as it advances from the highest memory address downward and expects to read a 1 in cell (2, 1) but instead receives a 0. MATS++ identifies the fault cell (2, 1) SA1. March element M1 detects the error as it advances from the lowest memory address upward and expects to read a 0 in cell (2, 1) but instead receives a 1.

M0: {March element $\updownarrow (w0)$ }
for cell: = 0 to n-1(or any other order) do
begin
write 0 to A [cell];
end;
M1: {March element $\uparrow (r0; w1)$ }
for cell: =0 to n-1 do
begin
read A [cell] ;{ Expected Value=0}
write 1 to A [cell];
end;
M2: {March element $\downarrow (r1; w0)$ }
for cell: = n-1 down to 0 do
begin
read A [cell]; {Expected Value=1}
write 0 to A [cell];
end;

Fig -2: MATS++ March Test Algorithm

When creating a memory utilising new technology, it is preferable to have a rapid yield learning curve. As a result, it is important to do highly extensive failure analysis using fault diagnosis in order to discover the specific problems (for example, it is essential to distinguish faults between SAF and CF). The end result of failure analysis is a new set of masks for the next fabrication cycle, which increases manufacturing yield. For the greatest process-specific fault coverage, a new set of March algorithms will be employed. To boost yield on big memory chips or SOCs with massive integrated SRAMs or DRAMs, it is critical to apply redundant memory placement methods. This sort of technique may be used to find the aggressor cell in a coupling failure, for example (CF).

4. SIMULATION RESULTS

The behavioural simulation of MUX_IN is shown in figure.3

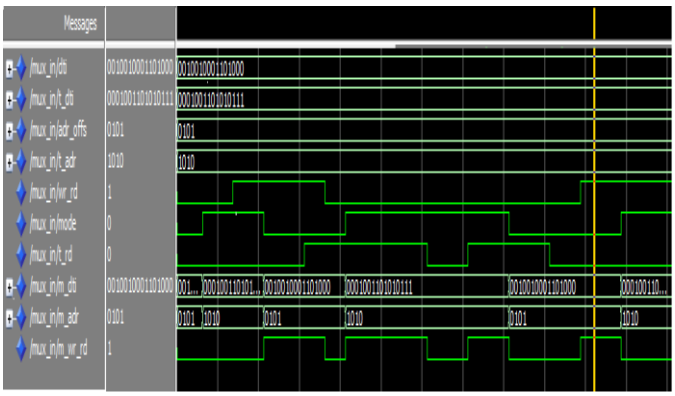

Fig -3: simulation waveform for the MUX_IN

The behavioural simulation for the MUX_OUT is shown in figure 4.

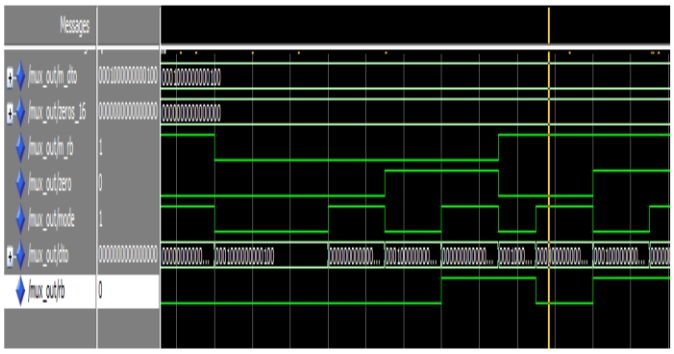

Fig -4: simulation waveform for the MUX_OUT

The behavioural simulation for the Memory Array is shown in figure 5.

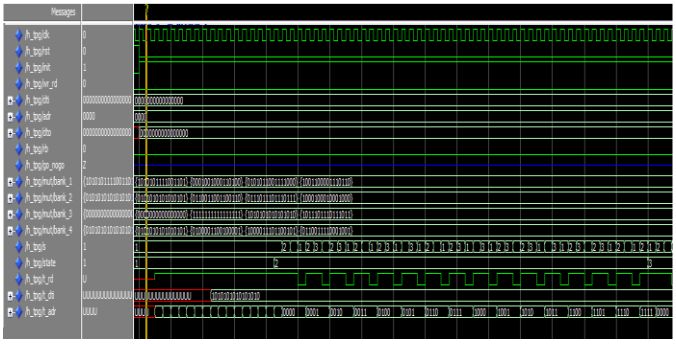

Fig -5: Memory Array

The behavioural simulation for the BIST_CTRL is shown in figure 6

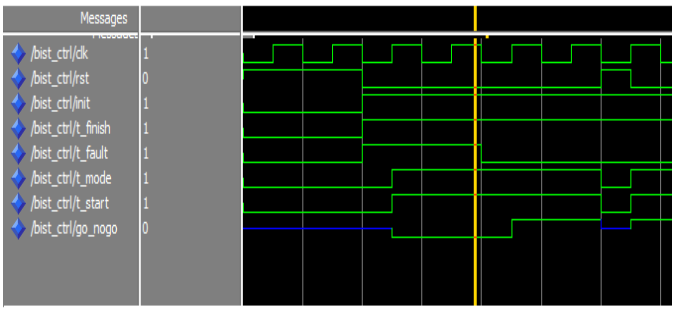

Fig -6: simulation waveform for the BIST_CTRL

The behavioural simulation for the MISR is shown in figure 7.

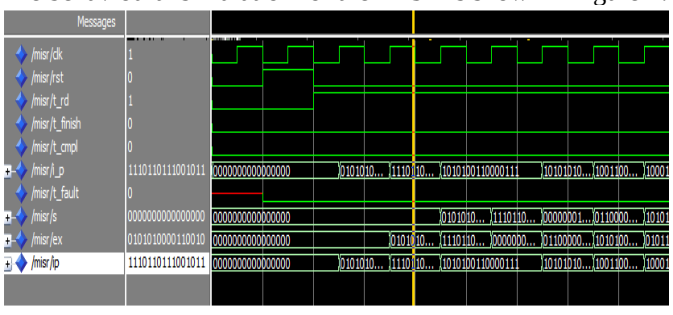

Fig -7: simulation waveform for the MISR

The behavioural simulation for the FSM with fault in the memory location is shown in figure 8.

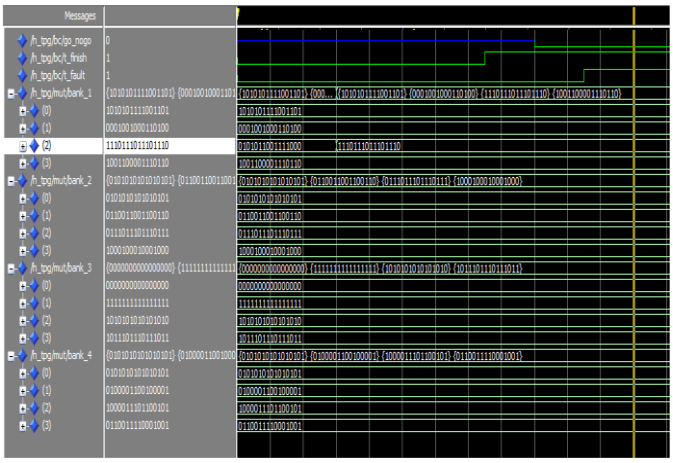

Fig -8: simulation waveform for the FSM with fault in the memory location

5. CONCLUSIONS

The novel approach takes advantage of transponders' idle status while waiting to be accessed by the interrogator to perform an internal memory test. The design of the transparent BIST circuit was given, as well as the transponder finite state machine explaining the access mechanism. The transparent March c- algorithm was created and successfully applied to evaluate RFID memory. Because of its better flexibility and extendibility in applying multiple combinations of memory test methods, this BIST is expected to be widely employed for embedded memory testing, particularly in the SOC design environment.

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